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(6) Applications of Analog Sampled Data Signal Processing to Low-Cost Speech Bandwidth Compression.

Professors (10) R. W. Brodersen

and P. R. Gray

(415) 642-1779

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

this contract

The basic objective of the NRL Contract N00173-77-C-0238 is to apply MOS-LSI techniques to the problem of narrow band vocoding. In particular, analog sampled data techniques are being used to implement the high speed processing required in an autocorrelation type linear predictive coder (LPC) and decoder. The remaining processing will then be performed in a relatively low speed (and therefore low cost) microprocessors. Also important in a complete narrow band vocoder is a pitch tracker. The method being investigated for this function is a modified version of the Gold-Rabiner time domain algorithm implemented using a hybrid analog-digital approach.

This report will be a brief summary of the present state of the work on the above three components of a complete LPC vocoder, which are shown inside the dashed lines in Fig. 1.

1) Linear Predictive Coder (LPC)

The autocorrelation approach[1] to LPC can be divided into two basic operations. The first is the calculation of the first ten autocorrelation coefficients. These coefficients are then used in a set of linear equations which are solved using the Levinson recursive algorithm.
The calculation of the autocorrelation coefficients requires relatively high speed processing since it must be performed at the speech sample rate (typically 8 kHz). The Levinson recursion, however, is only performed once every frame which is typically 10 to 20 milliseconds in length. Thus a partitioning of the system was chosen in which the autocorrelation coefficients are calculated using analog sampled data techniques and the Levinson recursion will be performed in a microprocessor.

The method used to implement the autocorrelation is indicated in Fig. 2. It is a classical analog method which was used before the advent of digital computers. However recently it has also been shown to have some advantages if the same organization is implemented digitally.[3] It is particularly well-suited to the analog sampled data techniques which have been recently investigated at Berkeley.[4,5]

The delay line (labeled D in the figure) is implemented using sample and hold circuits. The speech signal path that does not go through the delay line is A/D converted and is used as the digital input to the multipliers which are actually multiplying D to A converters. The A to D and D to A circuits use an algorithmic technique which only requires two MOS operational amplifiers and four MOS capacitors for the A to D and one op amp and two capacitors for the D/A.[6] The low pass filter will be implemented using switched capacitor techniques[5] which also only require a small amount of area.

The circuit has been computer simulated to determine if the accuracy which can be achieved using MOS techniques is adequate for stability of the Levinson recursion. The preliminary indications are that it is sufficient. A breadboard of this circuit is nearing completion and testing on the complete circuit will then begin.

2) Speech Synthesis Filter

The LPC synthesizer can be implemented as a ladder filter with time varying (programmable) coefficients. The ladder filters appear particularly amenable to implementation using switched capacitor techniques. In order to determine if there were any hidden difficulties in the ladder implementation a filter with fixed coefficients was fabricated and tested.[7] In Figs. 3 and 4 the integrated circuit is shown along with its frequency response. The filter was programmed with ratioed MOS capacitors to implement a five pole Chebychev response with 0.1 dB passband ripple. The dynamic range of this filter was in excess of 80 dB.

In order to make a programmable filter it is only necessary to replace the fixed capacitors with an array of capacitors that are switched in as required as shown in Fig. 5. The control of the analog filter chip is provided by a microprocessor which provides 10 digital words once each frame to update the filter. An investigation is now underway to determine the required number of capacitors in the arrays (the quantization) and their size in order to be compatible with existing LPC coders. It is expected a simple mapping will exist between LPC reflection coefficients and the switched capacitor ladder filter capacitor ratios.

3) Pitch Tracker

A modified version of the Gold-Rabiner algorithm which was developed by Bially and also modified by Blankenship is being breadboarded. The partitioning between analog and digital of this system is indicated in Fig. 6 . The analog section will implement the pre-filtering as well as the four elementary pitch trackers which are required in this algorithm. The scoring (pattern recognition) part of the algorithm will be performed in an Intel 8748 single chip microprocessor.

The microprocessor has been programmed and the breadboarding of the analog circuits is almost complete. It is expected that testing of the accuracy of the pitch tracker will begin within the next month.

Summary

All portions of a LPC vocoder are being either breadboarded or beginning IC design. The next major phase of work will involve evaluation of the breadboards and optimization of the partitioning and circuits. In addition, the design of an IC to perform the LPC synthesis is beginning.

References

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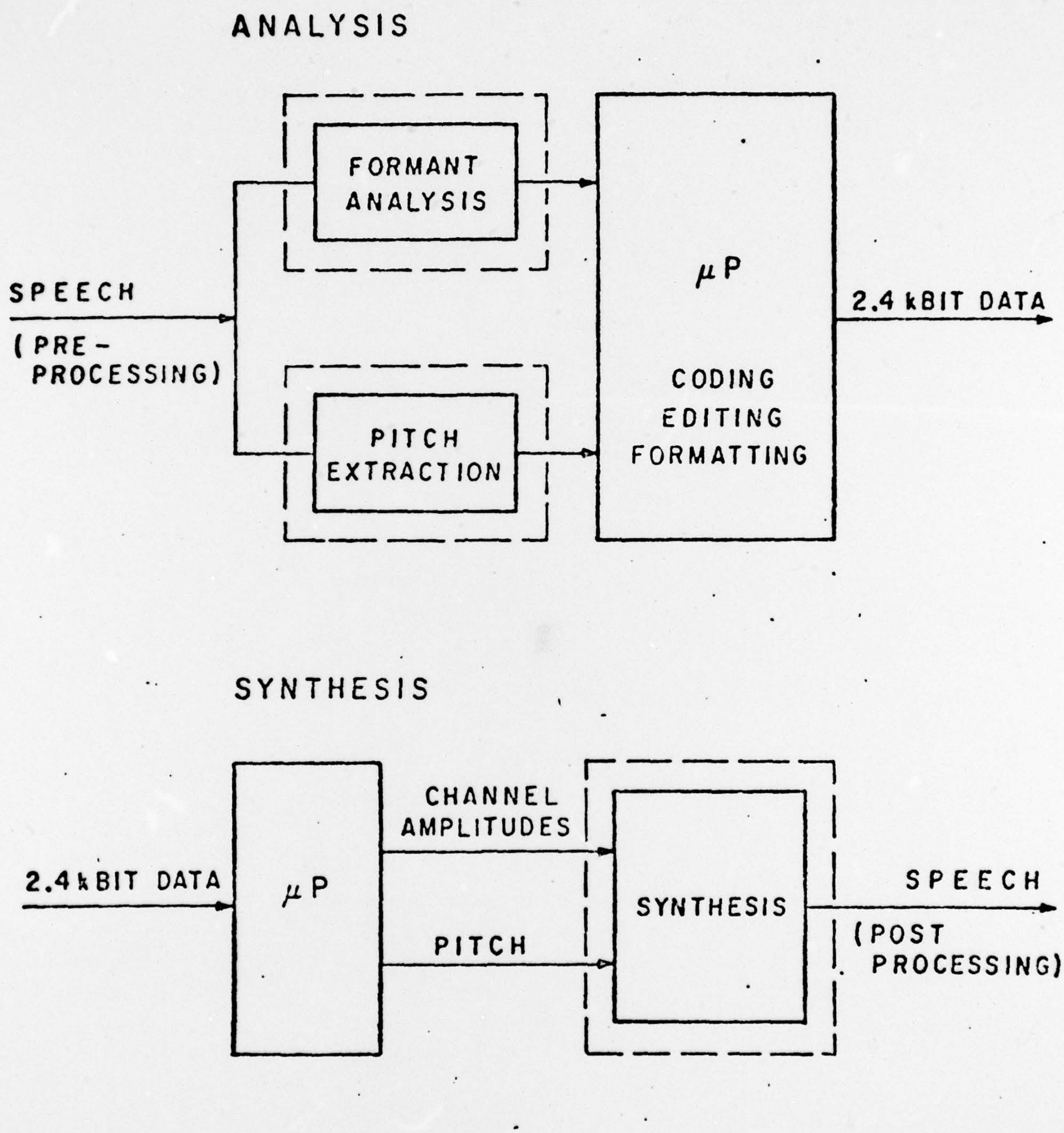

Fig. 1. A proposed block diagram of a complete vocoder system. The computations within the dashed lines are to be implemented using analog techniques on as few as three MOS-LSI chips.

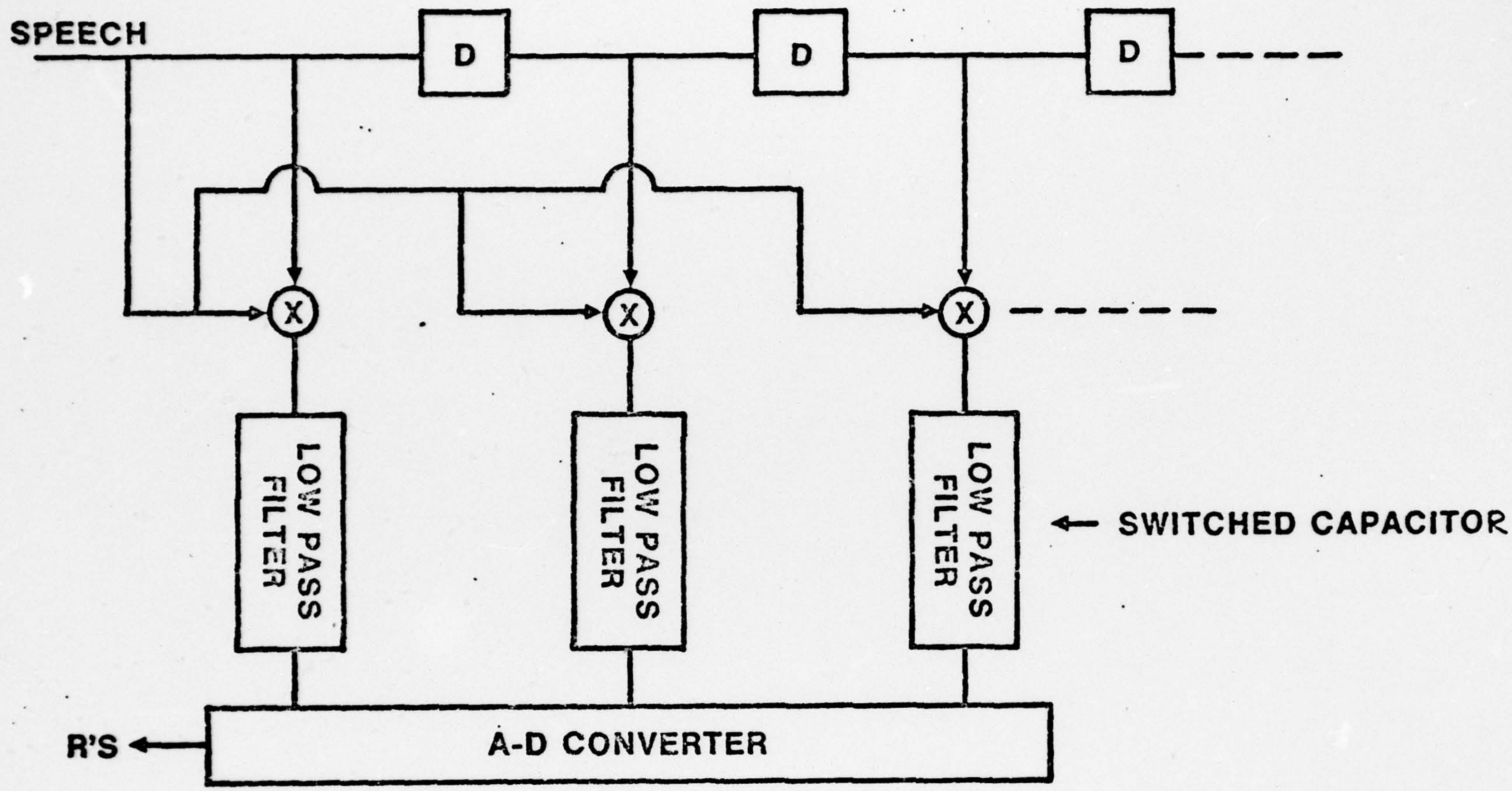
SPEECH
D
D
D
X
X
X
LOW PASS FILTER
LOW PASS FILTER
LOW PASS FILTER
SWITCHED CAPACITOR
A-D CONVERTER
R'S

Fig. 2

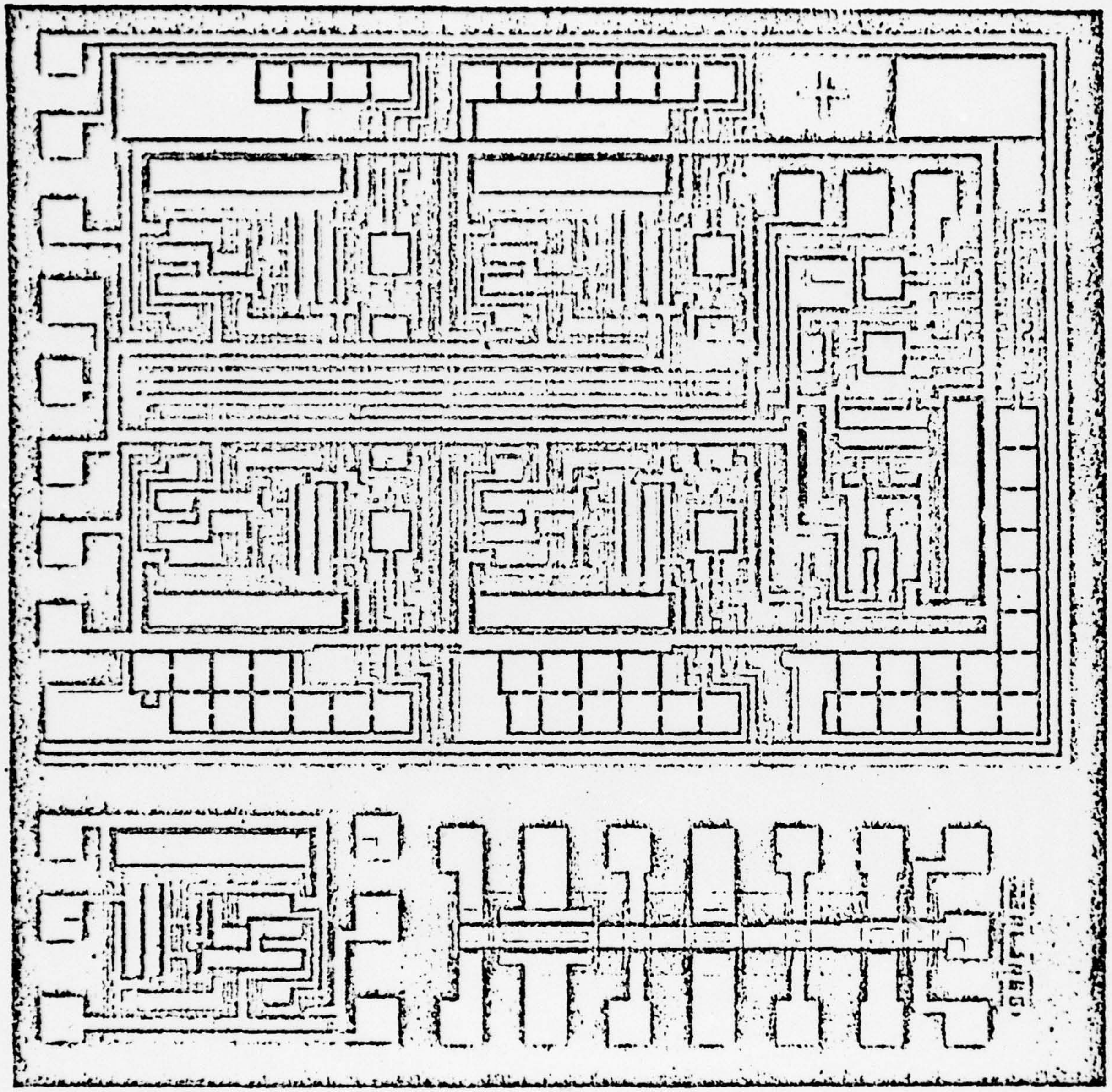

Fig. 3. Metal-gate NMOS circuit including fifth-order low-pass active-ladder filter. Overall die size is about 100 by 100 mils.

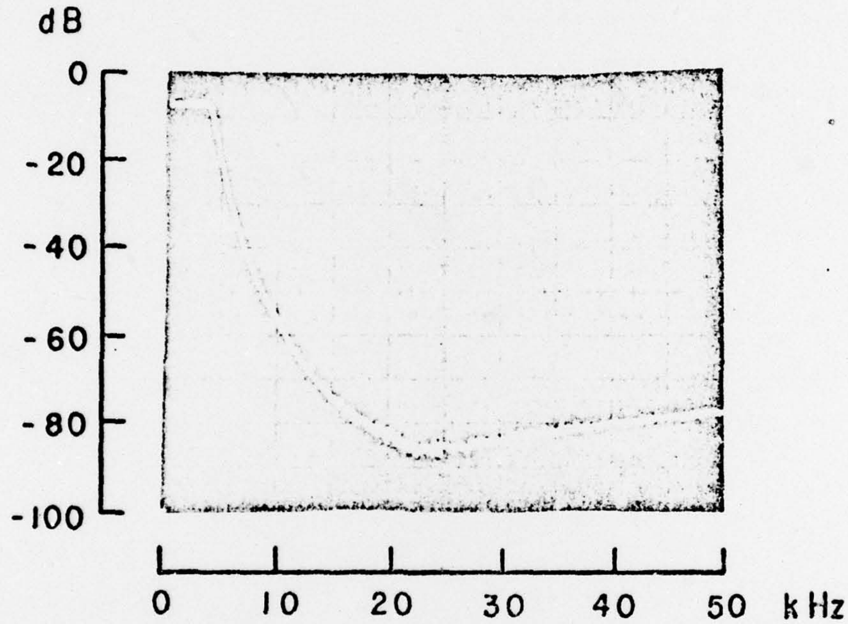

Fig. 4. Measured frequency response of Chebyshev fifth-order low-pass filter with 128 KHz sampling rate.

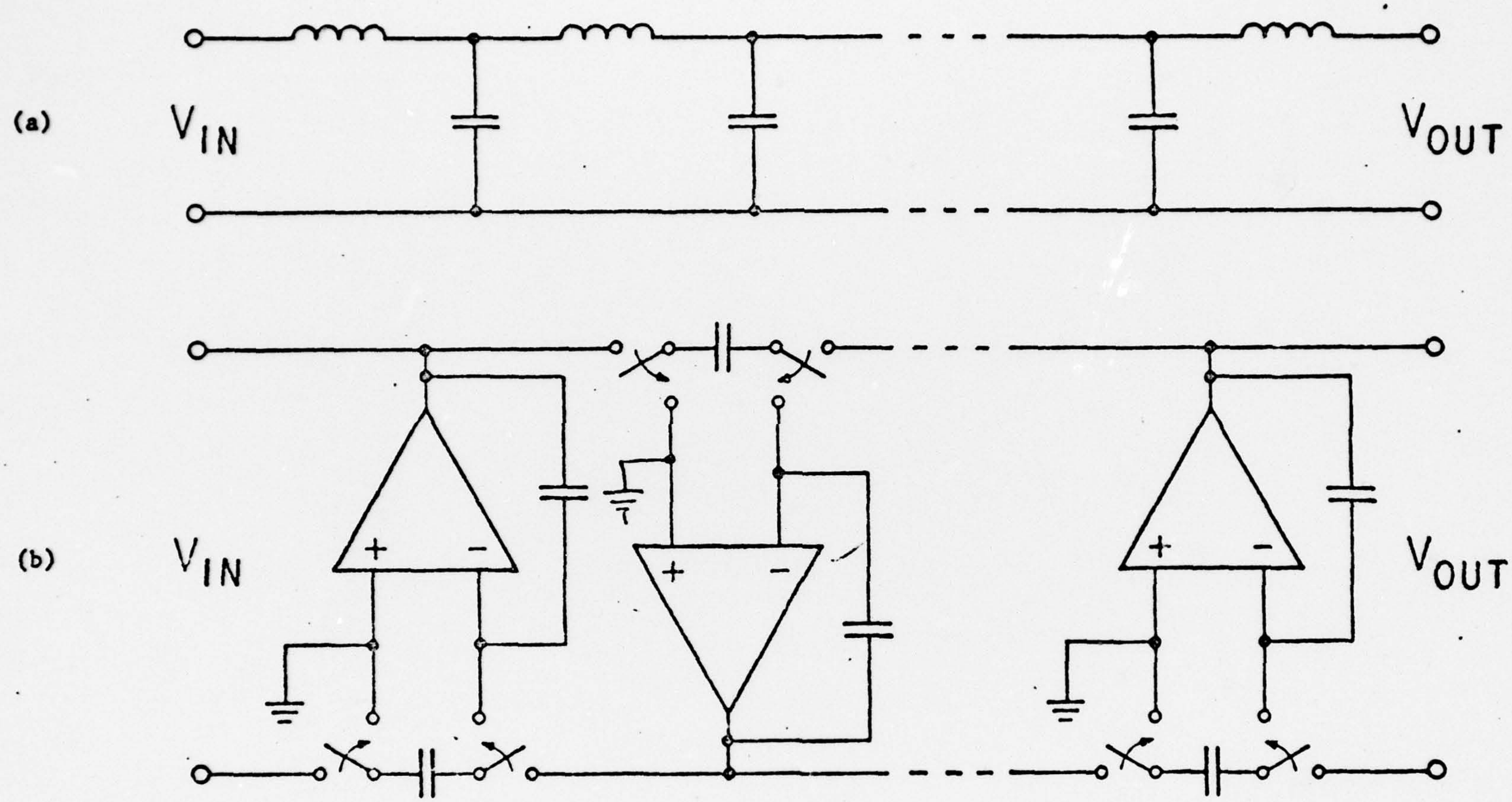

Fig. 5. (a) LC ladder filter for synthesis of a nonuniform acoustic tube; (b) A sampled data MOS version of the same filter.